MILADO

D8.1

First batch of twenty 8” Si wafers with surface nano-patterns and backside coating

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Abstract	This document describes the design and processing of silicon substrate. Those are with suitable architectures for direct epitaxial III-V – semiconductor growth.
Keywords	nano-structured surface of the Si substrate; direct epitaxial growth of III-V-semiconductors on silicon

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Executive Summary

This brief report is to accompany the delivery of deliverable (D) 8.1: “First batch of twenty 8” Silicon (Si) wafers with surface nano-patterns and backside coating”, which is of the “Demonstrator (DEM)” type. It describes the design and fabrication processing of this first batch. The obtained 20 wafers are with suitable architectures for direct epitaxial III-V –semiconductor growth.

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Chapter 1 Introduction

1.1 Context

The goal of work package (WP) 8 is the development of direct epitaxial growth of III-V-semiconductors on silicon towards monolithic integration of high-quality Quantum Cascade Laser (QCL). In contrast to the III-V-onto-Si bonding approach, which is limited by large-area III-V-substrate availability and the elaborate bonding process, the monolithic integration of III-V-semiconductors will greatly increase the manufacturing productivity and reduce device costs and feature size, enabling large volume market diagnostic devices. Facing challenges such as strain induced defect formation, anti-phase domains and different thermal expansion coefficients, which limit device performance and reliability, WP8 establishes measures for low defect III-V-growth, developing the Si-substrate architecture, processing and treatment, suitable epitaxial growth conditions and heterostructure design, and a profound structural analysis of the grown material. Emphasis lies in the compatibility with the existing complementary metal-oxide-semiconductor (CMOS) process technology for the full integrability in the high-volume manufacturing capabilities.

1.2 Description of work

Task 8.1 Design and processing of silicon substrates with suitable architectures for epitaxial III-V-semiconductor growth (M06-M28; Task Lead: CEA)
The direct growth of III-V-semiconductor on "plain" (001) Si is not favourable since the formation of strain-induced defects and anti-phase domains caused by monoatomic Si surface steps would severely limit the crystal quality of the III-V-material and thus device performance and reliability. The defect formation can be countered by a carefully designed, nano-structured surface of the Si substrate. In task (T) 8.1, a variety of different geometries will be developed together with Fraunhofer - Institut für Angewandte Festkörperphysik (FHG - IAF) and in total three batches of twenty 200 mm Silicon wafers will be processed and provided by CEA for the overgrowth at FHG - IAF in T8.2. Additionally, wafer backside coatings will be applied to counter act strain induced wafer deformation caused by the different lattice constants and thermal expansion coefficients of III-V-material and Si. Surface design and strain compensating measures with continuously by evaluated and adapted in T8.2.

Task 8.2 Development and analysis of the epitaxial growth of III-V-semiconductors on structured Si (M13-M28; Task Lead: FHG)
In T8.2, epitaxial growth of III-V-semiconductors is performed and analysed on the patterned substrates provided under T8.1. The quality of the material is strongly dependent on the substrate, the epitaxial growth conditions and the employed layer structure including measures for suppressed defect generation such as strain releasing buffers and defect filter layers. To analyse and optimize epitaxial layer quality, a simplified heterostructure suitable for easy-access epitaxial layer characterisation by high-resolution X-ray diffraction (HR-XRD), atomic force microscopy (AFM), and tunnelling electron microscopy (TEM) will be implemented. Iterative adjustments of the substrate geometry, substrate surface treatment, growth conditions and sample structure will be performed to successively reduce defect sites within the III-V-material. An additional focus lies on gaining a better understanding on different relevant defect generation mechanisms.

Task 8.3 Epitaxial growth of QCL heterostructures on Si and fabrication of a QCL test device (M29-M36; Task Lead: FHG)

Based on the insights gained in T8.2, established QCL test structures will be epitaxially grown on patterned 200 mm Si substrates and analysed using the structural analysis methods listed above. In order to perform electroluminescence measurements, an adapted process technology for structuring and contacting the QCL on Si will be developed and applied at FHG - IAF. These first measurements on electrical and electrooptical characteristics will enable insights into the specific device tolerances and relevant degradation processes to be considered towards the further development of the monolithic integration of QCL heterostructures on Si.

1.3 Role of participants in WP8

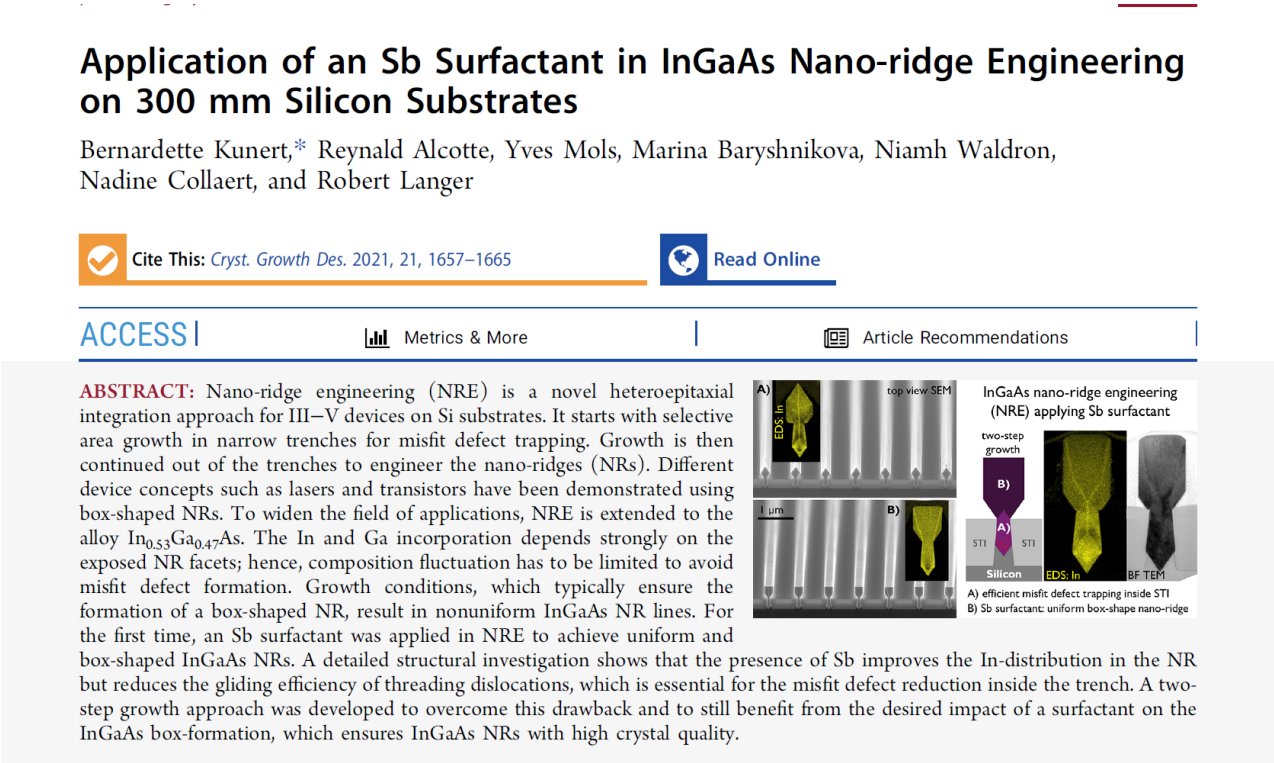
FHG develops the Si surface treatment, the epitaxial growth of III-V-semiconductor and QCL heterostructures on nano-patterned Si and performs the structural analysis, device processing and electroluminescence measurements. **CEA** develops and performs the nano-patterning process on 200 mm Si substrates based on the geometry designs developed together with FHG. Strained backside coating of the substrates will be implemented. In total, three batches of twenty 200 mm Silicon wafers will be provided for FHG.

D8.1	**First batch of twenty 8” Si wafers with surface nano-patterns and backside coating**	**WP8**	**CEA**	**DEM**	**PU**	**M08**
The required Si-substrates will be structured and provided by CEA according to the geometry and process developed together with IAF and will subsequently be overgrown with III-V-semiconductor material.						

Chapter 2 Design of silicon substrates

2.1 Bibliography

Technical exchanges between FHG – IAF and CEA-Leti led to the design of silicon substrates with suitable architectures for epitaxial III-V-semiconductor growth. This design is inspired from work performed in the Interuniversity Microelectronics Centre (IMEC). Figure 1 below shows a publication which inspired the used design.



Application of an Sb Surfactant in InGaAs Nano-ridge Engineering on 300 mm Silicon Substrates

Bernardette Kunert,* Reynald Alcotte, Yves Mols, Marina Baryshnikova, Niamh Waldron, Nadine Collaert, and Robert Langer

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ABSTRACT: Nano-ridge engineering (NRE) is a novel heteroepitaxial integration approach for III–V devices on Si substrates. It starts with selective area growth in narrow trenches for misfit defect trapping. Growth is then continued out of the trenches to engineer the nano-ridges (NRs). Different device concepts such as lasers and transistors have been demonstrated using box-shaped NRs. To widen the field of applications, NRE is extended to the alloy $In_{0.53}Ga_{0.47}As$. The In and Ga incorporation depends strongly on the exposed NR facets; hence, composition fluctuation has to be limited to avoid misfit defect formation. Growth conditions, which typically ensure the formation of a box-shaped NR, result in nonuniform InGaAs NR lines. For the first time, an Sb surfactant was applied in NRE to achieve uniform and box-shaped InGaAs NRs. A detailed structural investigation shows that the presence of Sb improves the In-distribution in the NR but reduces the gliding efficiency of threading dislocations, which is essential for the misfit defect reduction inside the trench. A two-step growth approach was developed to overcome this drawback and to still benefit from the desired impact of a surfactant on the InGaAs box-formation, which ensures InGaAs NRs with high crystal quality.

Figure 1: Snapshot of the scientific paper at the basis of the technology used in the present study.

2.2 Internal CEA-Leti know-how

In CEA-Leti, previous work was done by Laurence Andreutti and colleagues. The objective was to obtain an anisotropic etching of the Silicon with the solvent TMAH (TetraMethyl Ammonium Hydroxide, [(CH3)4NOH]). Figure 2 below shows the obtained results. The same process was used to prepare the wafers for D8.1.

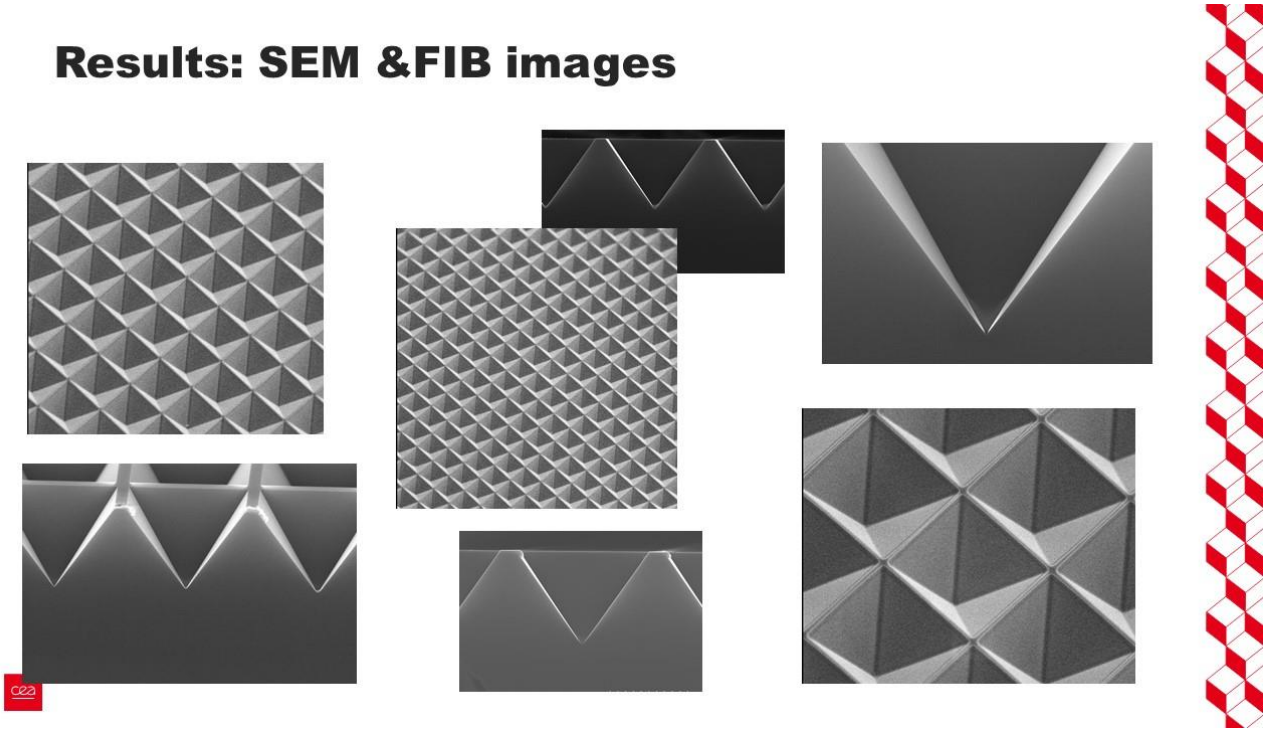

Figure 2: Snapshot of previous technology developed in CEA-Leti, work driven by Laurence Andreutti.

Chapter 3 Processing of silicon substrates

The colleagues working at FHG - IAF will perform direct epitaxy growth on the nanostructured wafer during the MILADO project. For this reason, a few variants were designed to investigate the impact of nanostructuring on the growth. Figure 3 and Figure 4 show the proposed variants. Feedback will be provided by FHG for further base wafers processing.

3.1 Base wafer preparation: design variants

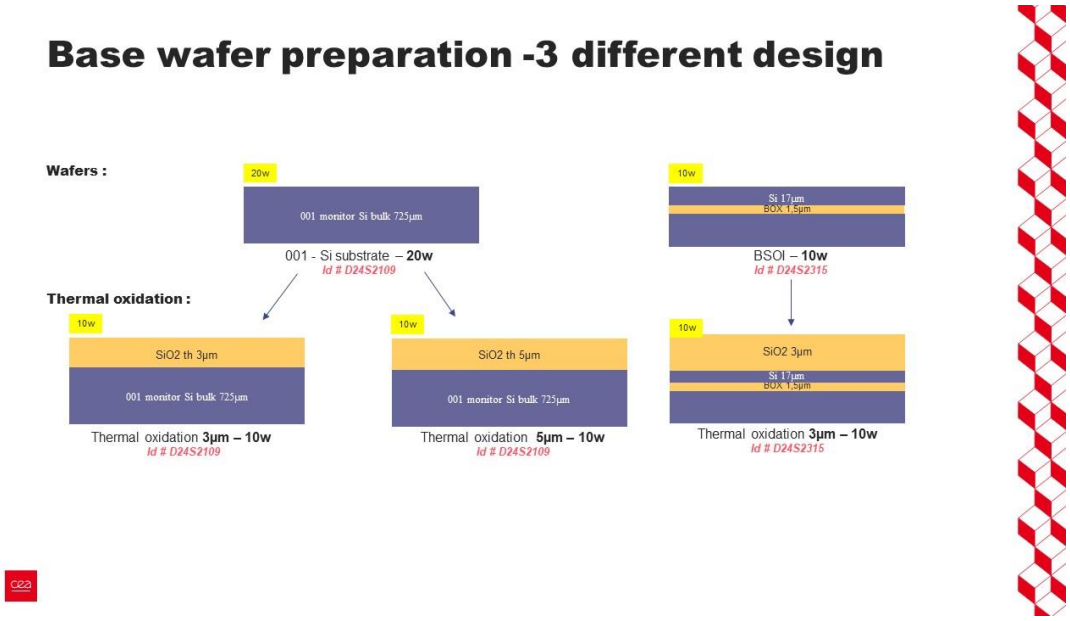

Figure 3: Design of variants for the wafers processing.

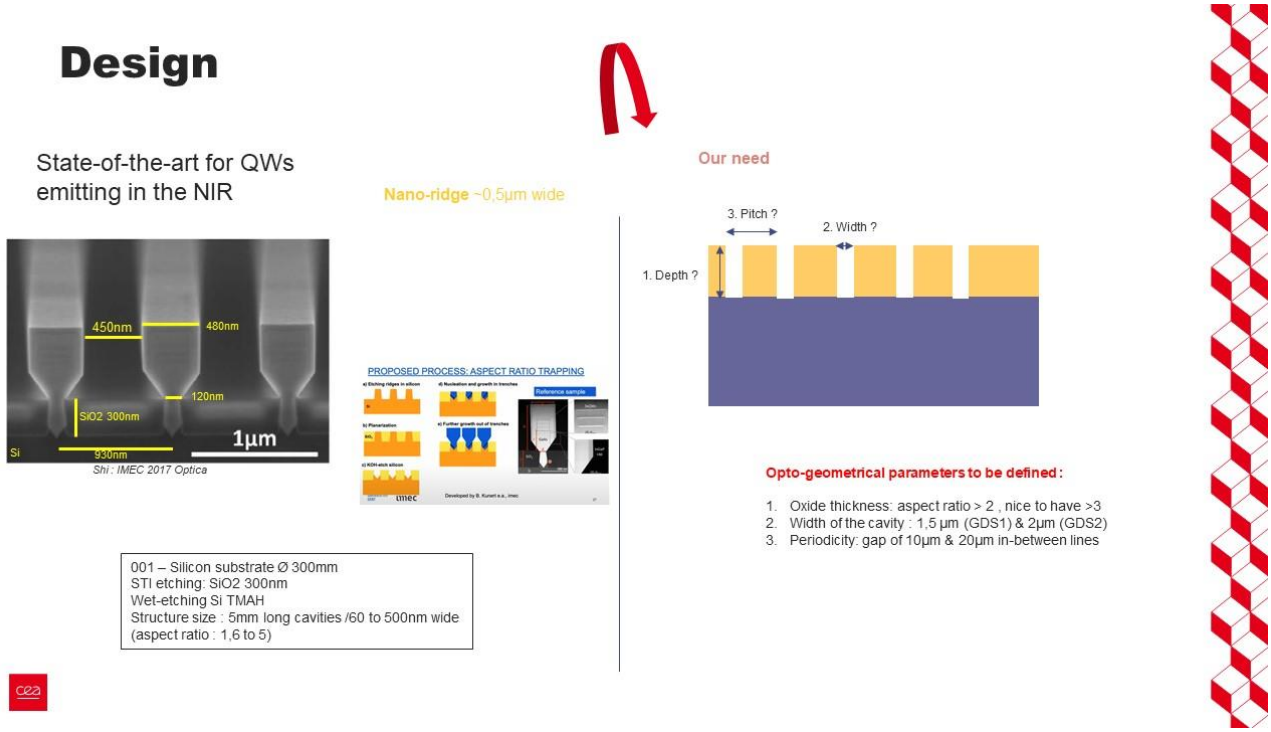

Figure 4: Opto-geometrical parameters were discussed with colleagues from FHG.

3.2 Base wafer preparation: mask design

Figure 5 and Figure 6 show the mask design necessary to obtain the desired nanostructure on the wafers, before they are processed for epitaxy at FHG - IAF.

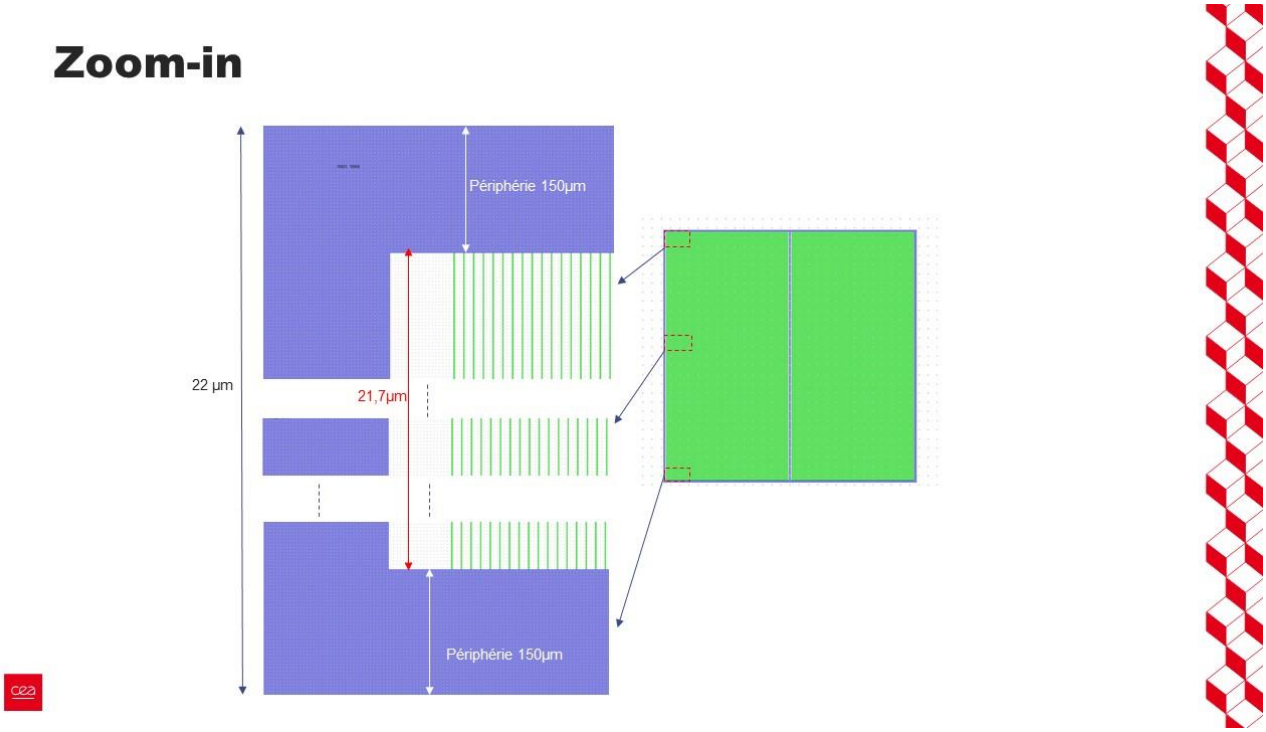

Figure 5: Zoom-in on one part of the field designed for the mask.

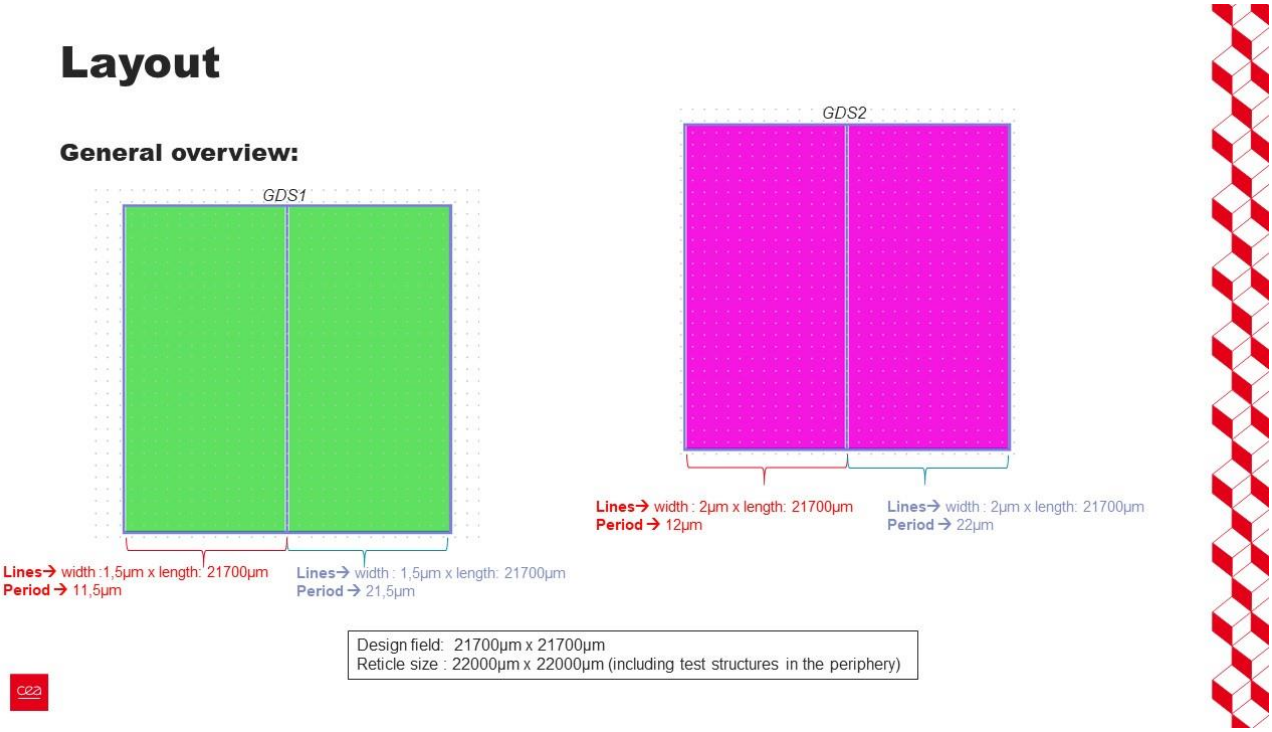

Figure 6: General view of the two masks used for the wafer processing

3.3 Base wafer preparation: fabrication result

We proceeded to the fabrication following the design plans exposed above. Figure 7 shows a focused ion beam (FIB) measurement performed after our first calibration. The cavity is filled with tungsten for the FIB measurement and to prevent from electronic charging in SiO_2. We observe a sharp triangle, and we also notice a lateral over-etch. For the next step, we will reduce the time from 1 hour to less than 30 minutes. This configuration can be seen as a new opportunity to be evaluated to break the dislocation vertically while maintaining the same SiO_2 aperture for the re-growth.

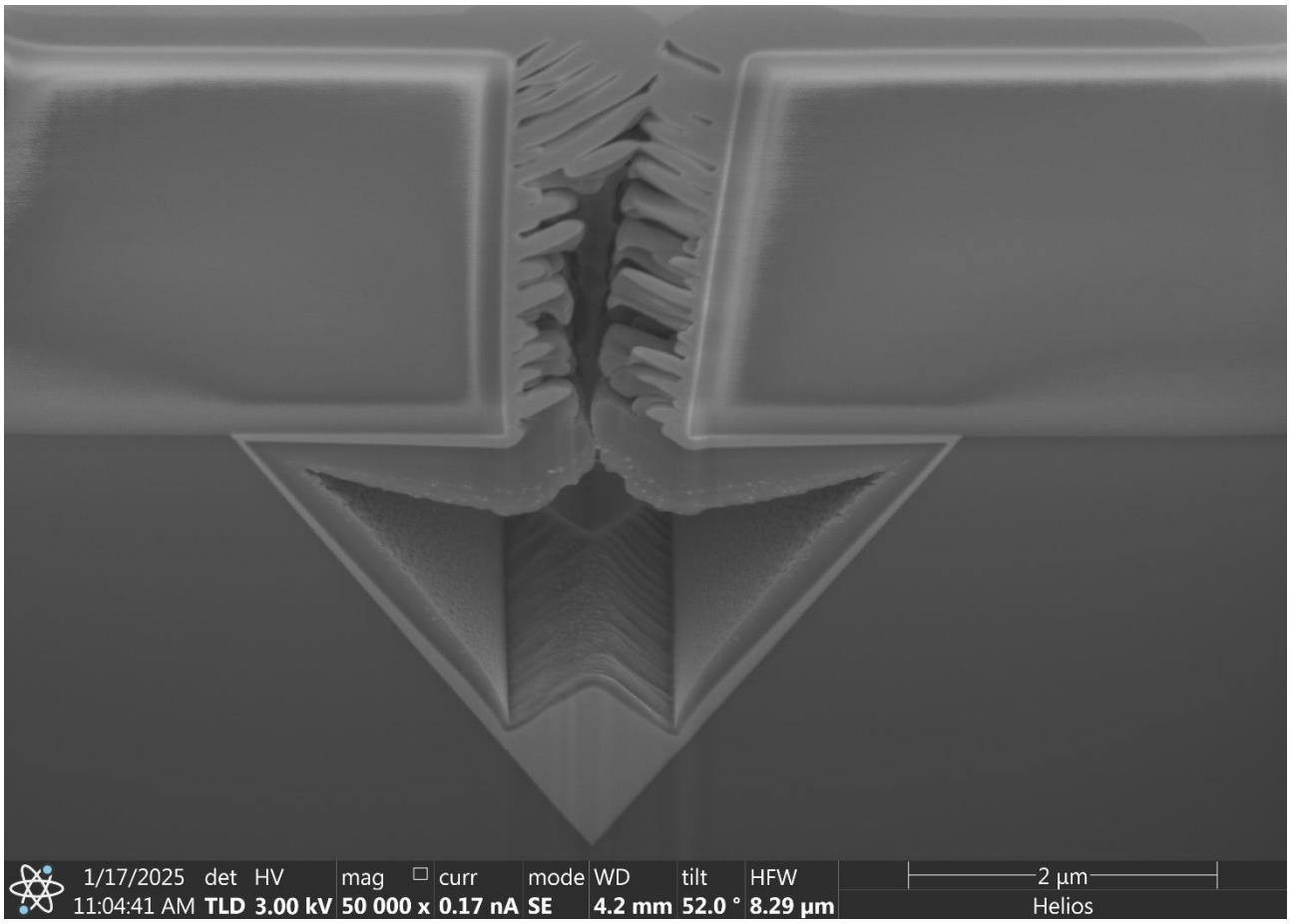

Figure 7: FIB measurement after the processing of one wafer

Chapter 4 Summary and conclusion

The goal of WP8 is the development of direct epitaxial growth of III-V-semiconductors on silicon towards monolithic integration of high quality QCL. Based on the literature results and internal know-how, CEA-Leti designed a process to perform nano-structuration on wafers. We detail the variants and the mask design. We obtained twenty wafers with nano-structuration. These wafers constitute D8.1 which is of the “Demonstrator” type.

Chapter 5 List of abbreviations

Abbreviation	Translation
AFM	Atomic force microscopy
CEA-Leti	Commissariat à l'énergie atomique et aux énergies alternatives - Laboratoire d'électronique et de technologie de l'information
CMOS	Complementary metal-oxide-semiconductor
D	Deliverable
DEM	Demonstrator
FHG-IAF	Fraunhofer-Institut für Angewandte Festkörperphysik
FIB	Focused ion beam
HR-XRD	high-resolution X-ray diffraction
IMEC	Interuniversity Microelectronics Centre
QCL	Quantum cascade laser
SEM	Scanning electron microscopy
Si	Silicon
T	Task
TEM	Tunnelling electron microscopy
TMAH	TetraMethyl Ammonium Hydroxide
WP	Work package